CLAIMS:

Please cancel claims 2, 3 and 8 and please replace claims 1, 4-7 and 9-12 with the following amended claims:

1. (Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is an integer ≧ 2) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer ≧ 2) gate selecting lines; and

{(N/M) + M} bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the gate of kth light-emitting thyristor is connected to ith [i ={(k-1) MOD M} +1] gate-electing ling G_i, where "MOD" in an equation means modulo division,

the anode or cathode which is not connected to the common terminal of the kth light-emiting thyristor is connected to jth [j = {(k-i)/M} + 1] anode terminal A_j or cathode terminal K_j, and

the number M of the gate-selecting lines is selected so as to satisfy the expression of L/{(N/M) + M} > p (L is a length of the long side of the chip and p is a critical value of the array pitch of the bonding pads) in order to decrease the area of the chip.

4. (Amended) The light-emitting thyristor matrix array of claim 1, wherein the critical value p of the array pitch of the bonding pads is about 75 μm.

5. (Amended) The light-emitting thyristor matrix array of claim 1, wherein when a prime factor for N is 2 only, the number M of the gate-selecting

lines is positive and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression $L/\{(N/M) + M\} > p$.

6. (Amended) The light-emitting thyristor matrix array of claim 1, wherein when prime factors for N are 2 and 3 only, the number M of the gate-selecting lines is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M) + M\} > p$.

7. (Amended) A light-emitting thyristor matrix array formed on a chip, comprising:

N (N is an integer $\geqq$ 2) three-terminal light-emitting thyristors arrayed in one line in parallel with the long side of the chip;

a common terminal to which cathodes or anodes of the N light-emitting thyristors are connected;

M (M is an integer $\geqq$2) anode-selecting lines or cathode-selecting lines; and

$\{(N/M)+M\}$ bonding pads arrayed in one line in parallel with the long side of the chip,

wherein the anode or cathode of kth light-emitting thyristor is connected to ith $[i=\{(k-1) \text{ MOD } M\} + 1]$ anode-selecting line A_i or cathode-selecting line K_i, where "MOD" in an equation means modulo division,

the gate of the kth light-emitting thyristor is connected to jth $[j=\{(k-i)/M\} + 1]$ gate terminal G_j and

the number M of the anode-selecting lines or cathode-selecting lines is selected to satisfy the expression of $L/\{(N/M)+M\} > p$ (L is a length of the long side of the chip and p is a critical value of array pitch of the bonding pads) in order to decrease the area of the chip.

Claim 8 has been canceled.

9. (Amended) The light-emitting thyristor matrix array of claim 7, wherein the critical value p of the array pitch of ~~the bonding pads~~ is about 75 μm.

10. (Amended) The light-emitting thyristor matrix array of claim 7, wherein when a prime factor for N is 2 only, M is positive and is the smallest integer, next smaller integer, or third smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

11. (Amended) The light-emitting thyristor matrix array of claim 7, wherein when prime factors for N are 2 and 3 only, M is positive and is the smallest integer, next smaller integer, third smaller integer, fourth smaller integer, or fifth smaller integer that satisfies the expression $L/\{(N/M)+M\}>p$.

12. (Amended) A driver circuit for driving the light-emitting thyristor matrix array according to any one of claims 1, 4, 5, and 6, comprising:

a circuit for driving the gate-selecting lines; and

a circuit for driving the anode terminals or cathodes terminal;

wherein the circuit for driving the gate-selecting lines including an even number of gate-selecting signal output terminals and a circuit for outputting a "selecting" signal to one of the gate-selecting signal output terminals and "no-selecting" signal to the others of the gate-selecting signal output terminals, with the terminal to which the "selecting" signal is supplied being switched in turn.